AMENDMENTS TO THE CLAIMS:

1-20 (Canceled)

21. (Currently amended) A system for transmitting multiple frames, each frame having a header field and a data field, for deep packet processing of the data field, said frames transmitted in a given sequence, for performing the deep packet processing on the data field of each of the frames, and for forwarding the processed frames to their destination in the same given sequence, comprising:

a) an input buffer for receiving frames for processing, having a buffer capacity of at least twice the size of the largest frame size, said buffer incorporated into a Data Moving Unit;

b) a Frame Header Processing Unit for determining the type of deep packet processing operation to be performed on each frame;

c) a plurality of processing core engines wherein each core engine has its own deep packet processing operation to be conducted on the data field of a frame, and an associated memory for storing a frame assigned to the engine until the engine is free to perform ~~a~~ said deep packet processing operation on the data field of the frame;

d) an arbitrator for assigning an ascending frame sequence number to each frame, for selecting a core engine based upon the type of operation to be performed on the data field of each frame, and for forwarding each frame to ~~one of~~ the selected core ~~engines~~ engine for deep-packet processing;

e) an output buffer for collecting each frame as it is processed by a core engine, said buffer having a buffer capacity of at least twice the size of the largest frame size and comprising a portion of the Data Moving Unit; and

f) a sequencer for forwarding processed frames from the output buffer to their destination in the same order as they are received by the input buffer.

22. (Currently amended) A method of transmitting multiple frames, each frame having a header field and a data field, to deep packet processing functions in a

given sequence, performing the deep packet processing on the data field of each frame and forwarding the processed frames to their destination in the same given sequence, comprising the steps of:

a) receiving frames into an input buffer that is incorporated into a Data Moving Unit, said buffer having a buffer capacity of at least twice the size of the largest frame size to be processed;

b) using a Frame Header Processing Unit to determine from the header field the type of deep packet processing operation to be performed on the data field of each frame;

c) assigning each frame to one of a plurality of processing core engines, based upon the processing operation to be conducted on the data ~~field of~~ contained in the frame, each frame being stored in a memory associated with a core engine until the engine is free to perform the processing operation on the data field of the frame;

d) performing at least one deep-packet processing operation on the data field in each frame;

e) collecting the processed frames in an output buffer that is incorporated into a Data Moving Unit, said buffer having a buffer capacity of at least twice the size of the largest frame size to be processed; and

f) sequencing and forwarding processed frames to their destination in the same order as said frames are received into the input buffer.

23. New) The system according to claim 21 including more than one core engine for a given type of deep packet processing operation, said arbitrator selecting which of the more than one core engines is to be used for said processing operation on a given frame.

24. (New) The method according to claim 22 including using more than one core engine for a given deep packet processing operation, said arbitrator selecting which of the more than one core engines is to be used for said processing of a given frame.

25. (New) The method according to claim 24 wherein the given frame is assigned from one deep packet operation to another by the arbitrator.

26. (New) The method according to claim 25 wherein separate paths are provided between core engines, and the given frame is transferred directly from the memory of one core engine into the memory of a second core engine.